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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/418,663	10/14/1999	James Robert Howard Hakewill	ARGONA.001A	9183

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EXAMINER	
GARCIA OTERO, EDUARDO	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 07/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/418,663	HAKEWILL ET AL.	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-22,40-42,47,48 and 60-117* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-22,40-42,47,48 and 60-117* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION: Final Action, after Request for Continued Examination

Introduction

1. Title is: METHOD AND APPARATUS FOR MANAGING THE CONFIGURATION AND FUNCTIONALITY OF A SEMICONDUCTOR DESIGN.
2. Applicants are: HAKEWILL et al.
3. This action is in response to Applicant's Amendments received 4/29/2004.
4. The pending claims are: 12-22, 40-42, 47-48, and 60-117.
5. The independent claims are: 12, 18, 40, 47, 48, 60, 75-79, 85, 91, 97, 102, 104, 106, and 108.
6. Applicant claims priority to provisional application 60/104,271 filed Oct. 14, 1998.

Index

7. **Dangelo'678** refers to Dangelo et al. US Patent 6,324,678 B1.
8. **Dupenloup'123** refers to Dupenloup et al. US Patent 6,378,123 B1.
9. **Wirthlin'434** refers to Wirthlin et al. US Patent 6,173,434.
10. **Dangelo'958** refers to Dangelo et al. US Patent 5,801,958.
11. **Rostoker'399** refers to Rostoker et al. US Patent 5,867,399.
12. **Cambell** refers to Cambell et al., "A tutorial for make", Proceedings of the 1985 ACM annual conference on the range of computing: mid-80's perspective, 1985, Denver, Colorado, United States. Pages 374-380. ISBN 0-89791-170-9.
13. **Gupte'474** refers to Gupte et al. US Patent 5,903,475.
14. **Heile'369** refers to Heile et al. US Patent 6,321, 369.
15. **Turino'892** refers to Turino et al. US Patent 5,994,892.
16. **Smith** refers to "HDL Chip Design" by Douglas J. Smith, Ninth printing July 2001, minor updates. First Printing June 1996. Doone Publications. ISBN 0-9651934-3-8. pages 1-25.

APPLICANT REMARKS

17. INTERVIEW AND POWERPOINT SLIDES. Said slides were visually presented at the personal interview of 3/26/04, and a printout was provided with Applicant's instant Amendment. Said slides were useful for clarifying some of the terminology issues from the prior office action. Now the written record is complete.

18. INFORMATION DISCLOSURE STATEMENT. The Examiner has amended and initialed the Information Disclosure Statement description of document #4 to include the date "1997" from the front page of the document. However the document #5 does not have any date. Please provide a date for this document #5 by Zanojnovic et al.
19. PREVIOUSLY PRESENTED CLAIMS. Applicant has substantially modified the previously presented claims. Thus, new rejections are presented below. Additionally, many new claims are presented for the first time, and are rejected below for the first time.
20. In addition to considering the new limitations, note that the rejections have been simplified (or consolidated) by using Dangelo'678 for more of the limitations. Further note that the "automated" limitations are addressed explicitly through reference to MPEP 2144.04. These simplifications reduce or eliminate reliance upon Gupte and Dupenloup.
21. PETER HUTTON DECLARATION. Applicant's declaration by Peter Hutton provides some evidence of commercial success, and is given some weight. However, said declaration is not give great weight for several reasons. First, there is not a clear mapping between the limitations of the claims to the elements of the commercially successful product. Declaration section 6 recites the limitations of claim 12, but does not map them to the elements of the commercial product through a user's manual or other documentation.
22. Note that the prior office action paragraph 261 stated "The Examiner requests the following: (1) the **earliest User's Manual for the Architect™** product which is the embodiment of the instant claimed invention, including a mapping of claim limitations to the product features, (2) all relevant information regarding the **first publication, public use, or sale of said product.**" Emphasis in original. No such user's manual or mapping has been provided. Such documentation would be strong evidence supporting commercial success, but has not been provided. Further, if commercial success is asserted, then that implicitly raises the issue of potential statutory bars, if sold or offered for sale more than one year before the effective filing date, see 35 USC 102(b).
23. Second, there is not a clear nexus between the claimed invention and the (undisputed) evidence of commercial success. Basically, it is not clear that the success of the commercial product is due to the claimed invention, and not due to other reasons. See MPEP 716.03.

24. Third, the statement in the declaration section 8 "there was an unsolved need" is a legal conclusion, and is not evidence supporting said conclusion. Contrast with *Minnesota Mining and Manufacturing Co. v. Johnson & Johnson Orthopedics, Inc.*, 24 USPQ 2d 1321 (Fed. Cir. 1992). In *Minnesota Mining*, the evidence supporting an "unsolved need" included a license issued to a competitor who had failed to make a similar product with different material (see pages 1333-1335).
25. However, the commercial success in sections 9-14 is substantial, and there is some evidence that said success may be least partially due to the claimed invention. Thus, the Peter Hutton declaration is given some weight, but not great weight. Compare with the powerful and colorful evidence in *Minnesota Mining*.

35 USC § 112-Second Paragraph-indefinite claims

26. The following is a quotation of the second paragraph of 35 U.S.C. 112: The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
27. **Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite** for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
28. In claim 12 (currently amended), the term "library files that provide at least one prototype description and at least one extension logic description" is not adequately defined. Note that specification page 16 states "file extensions... extensions library files... extensions include core registers, ALU extensions that provide more operations, auxiliary registers..." Claim 12 appears to be related to the page 16 file extensions, but the terminology is inconsistent. Further, it is not clear how the claim term "prototype description" is different from "extension logic description". Please clarify the definitions of these terms.

Claim Rejections - 35 USC § 103

29. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action: A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

30. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: Determining the scope and contents of the prior art. Ascertaining the differences between the prior art and the claims at issue. Resolving the level of ordinary skill in the pertinent art. Considering objective evidence present in the application indicating obviousness or nonobviousness.

31. **Claims 12-22, 40-42, 47-48, and 60-117 are rejected under 35 U.S.C. 103(a) as being unpatentable.**

32. Claim 12 (currently amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of MPEP 2144.04(III) Legal Precedent.

33. Claim 12 is in independent claim with 9 limitations.

34. [1]-**"creating a customized description language model of an integrated circuit design by: receiving one or more inputs from a user for at least one customized parameter of the integrated circuit"** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL", and at FIG 2 showing iterative modifications to the design.

35. [2]-**"receiving an identification of a location of one or more library files that provide at least one prototype description and at least one extension logic description for the integrated circuit for which a model is being generated"** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL", and column 9 line 29 "Design Description. This is the functional description of the design and all its subsystem elements. The description is, ideally, given in a high level description language, such as VHDL. Depending on the nature of the design, the description can be entirely at the behavioral level, or it may be intertwined with an RTL description", and column 9 line 1 "The mega-cell and mega-function block 116 is chosen from pre-designed building block libraries, which are already designed for optimal performance" and FIG 12 "PREDESIGNED BLOCKS", and FIG 8 element 818 "LIBRARIES", and FIG 18 element 1810 "COMPONENT DATABASE".

36. [3]-**"...a customized description language model based on at least one customized parameter, the at least one prototype description, and the at least one extension logic description, the automated process including the acts of reading at least one prototype**

description and modifying the at least one prototype a description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one customized parameter" is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL", and at FIG 2 showing iterative modifications to the design. Note that iterative modifications are equivalent to substituting values or merging additional descriptions.

37. [4]-**"generating a netlist which is descriptive of the circuitry of said integrated circuit"** is idisclosed by Dangelo'678 at Column 49 line 56 "compiling and simulating the netlist".
38. [5]-**"compiling said netlist and said hardware description model to produce a compiled integrated circuit design"** is disclosed by Dangelo'678 at Column 49 line 56 "compiling and simulating the netlist".
39. [6]-**"fabricating at least one mask or FPGA configuration file representing said compiled integrated circuit design"** is disclosed by Dangelo'678 at Column 41 line 59 "mask level".
40. [7]-**"fabricating said integrated circuit using said at least one mask or FPGA configuration file"** is disclosed by Dangelo'678 at Column 41 line 59 "mask level". Note that the purpose of mask is to fabricate a circuit corresponding to the mask.
41. [8]-**"wherein said act of creating is performed at a high level of abstraction"** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL", and at FIG 2 showing iterative modifications to the design.
42. Dangelo does not explicitly disclose the additional limitations.
43. [9]-**"generating through an automatic process..."** is disclosed by MPEP 2144.04(III) Legal Precedent. *In re Venner*, 262 F.2d 91, 95, 120 USPQ 192, 194 (CCPA 1958) states "it is well settled that it is not "invention" to broadly provide a mechanical or automatic means to replace manual activity which has accomplished the same result." Additionally, MPEP 2144.04(III) states "broadly providing an automatic or mechanical means to replace a manual activity which accomplished the same result is not sufficient to distinguish over the prior art."

44. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use MPEP 2144.04(III) Legal Precedent to modify Dangelo'678. One of ordinary skill in the art would begin with Dangelo as a basis for designing integrated circuits, and then would be motivated to save time and money by carefully documenting and saving modules of building blocks, or medium sized circuits that can be used repeatedly as building blocks for large designs. Note that this is analogous to using "libraries" of gate level components, rather than repeatedly designing similar gate level components. Additionally, one of ordinary skill in the art would be motivated to save time and money (and reduce error) by automating the repetitive steps of reading, substituting, or merging the relevant building blocks.
45. Claim 13 (currently amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 and MPEP 2144.04(III) Legal Precedent and Wirthlin'434.
46. Claim 13 (currently amended) depends from Claim 12 (currently amended), with four additional limitations.
47. **(ii)-"cache configurations"** is disclosed by Dangelo'678 at Column 9 line 25 "functional specifications of subsystem elements", and Dangelo'678 at Column 13 line 37 "memory, mega-cells, mega-functions".
48. **(iii)-"memory interface configurations"** is disclosed by Dangelo'678 at Column 9 line 27 "interface requirements".
49. **(iv)-"system architecture configurations"** is disclosed Dangelo'678 at Column 43 line 55 "architecture synthesis system".
50. Dangelo'678 does not expressly disclose custom instruction sets.
51. **(i)-custom instruction sets"** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".
52. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use MPEP 2144.04(III) Legal Precedent and Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would begin with Dangelo'678 as a basis for designing integrated circuits, and then would be motivated to save time and money by carefully documenting and saving modules of building blocks, or medium sized circuits that

can be used repeatedly as building blocks for large designs. Note that this is analogous to using technology specific "libraries" of gate level components (primitives), rather than repeatedly designing similar gate level components. Additionally, one of ordinary skill in the art would be motivated to save time and money (and reduce error) by automating the repetitive steps of reading, substituting, or merging the relevant building blocks, and to motivated to allow "additional cycles for instructions that need significantly more time than traditional low-level instructions" according to Wirthlin'434 at Column 10 line 36, and to fabricate the design that Dangelo'678 produced.

53. Claims 14-17 (currently amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of MPEP 2144.04(III) Legal Precedent and Dupenloup'123 and Dangelo'958.
54. Claims 14-17 depend directly or indirectly from claim 12.
55. In claim 14, "**generating a list of logic devices and their interconnections**" is disclosed by Dangelo'678 at Column 49 line 55 "creating a netlist".
56. In claim 15, "**defining physical features on a semi-conductive substrate via a lithographic process** is disclosed by Dupenloup'123 at Column 79 line 58 to Column 80 line 1 "Photolithography... semiconductor material".
57. In claim 16, "**synthesizing said design based on said description language model**" is disclosed by Dangelo'678 at Column 4 line 6 "logic synthesis".
58. In claim 17, "**receiving inputs is performed interactively with the user using a display**" is disclosed by Dangelo'958 at Column 10 line 45 "user input occurs by pointing with the pointing device and selecting connection nodes, nets or devices and issuing commands which affect the selected object's numerical parameters". Note that Dangelo'958 "point and select" inherently discloses: a display, a pointer, and related graphical user interface software. Dangelo's "point and select" precisely discloses interactive editing (which inherently includes receiving inputs), where the user interacts with a display using a pointer and related software.
59. MOTIVATION FOR CLAIMS 14-17. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use MPEP 2144.04(III) Legal Precedent and Dupenloup'123 and Dangelo'958 to modify Dangelo'678. One of ordinary

skill in the art would begin with Dangelo'678 as a basis for designing integrated circuits, and then would be motivated to save time and money by carefully documenting and saving modules of building blocks, or medium sized circuits that can be used repeatedly as building blocks for large designs. Note that this is analogous to using technology specific "libraries" of gate level components (primitives), rather than repeatedly designing similar gate level components. Additionally, one of ordinary skill in the art would be motivated to save time and money (and reduce error) by automating the repetitive steps of reading, substituting, or merging the relevant building blocks, and to motivated to allow "additional cycles for instructions that need significantly more time than traditional low-level instructions" according to Wirthlin'434 at Column 10 line 36, and to fabricate the design that Dangelo'678 produced. One of ordinary skill in the art would have been motivated to do this to fabricate the design that Dangelo'678 produced, and to facilitate the user interaction with the editing program. Graphical user interfaces including "point and click" menus are universally recognized as efficient ways to interact with computers. For example, graphical user interfaces including a pointing mouse and clicking menus have been standard even on cheap personal computers for approximately 8 years.

60. Claim 18 (Currently amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.
61. Claim 18 (presently amended) is an independent "apparatus" claim with 7 limitations.
62. [4]-"**a computer program resident at least in part on said storage device, said computer program adapted to perform the following acts: receiving one or more inputs from a user for at least one customized parameter of the integrated circuit**" is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL", and column 9 line 29 "Design Description. This is the functional description of the design and all its subsystem elements. The description is, ideally, given in a high level description language, such as VHDL. Depending on the nature of the design, the description can be entirely at the behavioral level, or it may be intertwined with an RTL description", and column 9 line 1 "The mega-cell and mega-function block 116 is chosen from pre-designed building block libraries, which are already

designed for optimal performance" and FIG 12 "PREDESIGNED BLOCKS", and FIG 8 element 818 "LIBRARIES", and FIG 18 element 1810 "COMPONENT DATABASE".

63. [5]-"**receiving an identification of a location of one or more library files that provide at least one prototype description and at least one extension logic description for the integrated circuit for which a model is being generated"** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL", and column 9 line 29 "Design Description. This is the functional description of the design and all its subsystem elements. The description is, ideally, given in a high level description language, such as VHDL. Depending on the nature of the design, the description can be entirely at the behavioral level, or it may be intertwined with an RTL description", and column 9 line 1 "The mega-cell and mega-function block 116 is chosen from pre-designed building block libraries, which are already designed for optimal performance" and FIG 12 "PREDESIGNED BLOCKS", and FIG 8 element 818 "LIBRARIES", and FIG 18 element 1810 "COMPONENT DATABASE".
64. [6]-"**generating a customized description language model based on at least one customized parameter, the at least one prototype description, and the at least one extension logic description, the automated process including the acts of reading at least one prototype description and modifying the at least one prototype a description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one customized parameter"** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL", and at FIG 2 showing iterative modifications to the design. Note that iterative modifications are equivalent to substituting values or merging additional descriptions.
65. Dangelo'678 does not expressly disclose processor, storage device, and input device.
66. [1]-"**a processor capable of running a computer program"** is disclosed by Dupenloup'123 at FIG 46 element 952 MICROPROCESSOR.
67. [2]-"**a storage device being capable of storing at least a portion of a computer program"** is disclosed by Dupenloup'123 at FIG 46 element 958 MASS STORAGE.

68. [3]-"**an input device, operatively coupled to said processor, capable of receiving input from a user and transmitting said input to said processor**" is disclosed by Dupenloup'123 at FIG 46 element 964 INPUT DEVICE.
69. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to Dupenloup'123 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to make the Dangelo'678 design process faster, cheaper, and with less errors by using computers instead of pencil and paper.
70. Claims 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.
71. Claims 19-22 depend directly or indirectly from independent claim 18.
72. In claim 19, "**said description language model is a hardware description language (HDL)**" is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL".
73. In claim 20, "**generating a file based on said description language model for use with a simulation**" is disclosed by Dangelo'678 at Column 1 line 53 "information necessary for layout, verification and simulation into a schematic object file or files".
74. Also in claim 20, "**simulating said design using said file**" is disclosed by Dangelo'678 at Column 1 line 61 "generates a set of simulation results".
75. In claim 21, "**running synthesis scripts based on said description language model in order to synthesize said integrated circuit design**" is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".
76. In claim 22, "**said processor comprises a digital microprocessor**" is disclosed by Dupenloup'123 at FIG 46 element 952 MICROPROCESSOR.
77. Also in claim 22, "**said storage device comprises magnetic media**" is disclosed by Dupenloup'123 at FIG 46 element 958 MASS STORAGE. Note that magnetic media is the most common method of mass storage.
78. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to Dupenloup'123 to modify Dangelo'678. One of ordinary skill in the art would

have been motivated to do this to make the Dangelo'678 design process faster, cheaper, and with less errors by using computers instead of pencil and paper.

79. Claim 40 (currently amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

80. Claim 40 is an independent "system" claim (or "machine" per 35 USC 101), with 5 limitations.

81. [3]-**"an input receiving module that receives one or more inputs from a user for at least one customized parameter of an integrated circuit device, the at least one customized parameter comprising a parameter selected from a group comprising a custom instruction, a cache configuration, a memory interface configuration and a system architecture configuration"** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL", and at FIG 2 showing iterative modifications to the design ,and column 9 line 29 "Design Description. This is the functional description of the design and all its subsystem elements. The description is, ideally, given in a high level description language, such as VHDL. Depending on the nature of the design, the description can be entirely at the behavioral level, or it may be intertwined with an RTL description", and column 9 line 1 "The mega-cell and mega-function block 116 is chosen from pre-designed building block libraries, which are already designed for optimal performance" and FIG 12 "PREDESIGNED BLOCKS", and FIG 8 element 818 "LIBRARIES", and FIG 18 element 1810 "COMPONENT DATABASE".

82. [4]-**"a library file receiving module that receives an identification of a location of one or more library files that provide at least one prototype description and at least one extension logic description for the integrated circuit device for which a model is being generated"** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL", and at FIG 2 showing iterative modifications to the design ,and column 9 line 29 "Design Description. This is the functional description of the design and all its subsystem elements. The description is, ideally, given in a high level description language, such as VHDL. Depending on the nature of the design, the description can be entirely at the behavioral level, or it may

be intertwined with an RTL description", and column 9 line 1 "The mega-cell and mega-function block 116 is chosen from pre-designed building block libraries, which are already designed for optimal performance" and FIG 12 "PREDESIGNED BLOCKS", and FIG 8 element 818 "LIBRARIES", and FIG 18 element 1810 "COMPONENT DATABASE".

83. [5]-**"a generation module that generates a customized description language model based on at least one customized parameter, the at least one prototype description. and the at least one extension logic description through acts including reading at least one prototype description and modifying the at least one prototype description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one customized parameter"** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL", and at FIG 2 showing iterative modifications to the design ,and column 9 line 29 "Design Description. This is the functional description of the design and all its subsystem elements. The description is, ideally, given in a high level description language, such as VHDL. Depending on the nature of the design, the description can be entirely at the behavioral level, or it may be intertwined with an RTL description", and column 9 line 1 "The mega-cell and mega-function block 116 is chosen from pre-designed building block libraries, which are already designed for optimal performance" and FIG 12 "PREDESIGNED BLOCKS", and FIG 8 element 818 "LIBRARIES", and FIG 18 element 1810 "COMPONENT DATABASE".
84. Dangelo'678 does not explicitly disclose the additional limitations.
85. [1]-**"a processor"** is disclosed by Dupenloup'123 at FIG 46 element 952 MICROPROCESSOR
86. [2]-**"a storage device in data communication with said processor"** is disclosed by Dupenloup'123 at FIG 46 element 956 RAM.
87. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to Dupenloup'123 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to make the Dangelo'678 design process faster, cheaper, and with less errors by using computers instead of pencil and paper.

88. Claim 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 and Dupenloup'123 and Gupte.
89. Claim 41-42 depend directly or indirectly from independent claim 40.
90. In claim 41, "**plurality of process technology options**" is disclosed by Gupte at Column 4 line 60 "process technology".
91. In claim 42, "**pre-configured data file**" is disclosed by disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL", and at FIG 2 showing iterative modifications to the design ,and column 9 line 29 "Design Description. This is the functional description of the design and all its subsystem elements. The description is, ideally, given in a high level description language, such as VHDL. Depending on the nature of the design, the description can be entirely at the behavioral level, or it may be intertwined with an RTL description", and column 9 line 1 "The mega-cell and mega-function block 116 is chosen from pre-designed building block libraries, which are already designed for optimal performance" and FIG 12 "PREDESIGNED BLOCKS", and FIG 8 element 818 "LIBRARIES", and FIG 18 element 1810 "COMPONENT DATABASE".
92. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to Dupenloup'123 and Gupte to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to make the Dangelo'678 design process faster, cheaper, and with less errors by using computers instead of pencil and paper, and to organize separate libraries for each technology in order to reduce potential errors from mixing technologies.
93. Claim 47 (currently amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Gupte and Wirthlin'434.
94. Claim 47 (currently amended) is an independent "method".
95. [3]-"**(ii) cache configuration**" is disclosed by Dangelo'678 at Column 9 line 25 "functional specifications of subsystem elements", and Dangelo'678 at Column 13 line 37 "memory, mega-cells, mega-functions" (and also is disclosed by Dupenloup'123 at Column 78 line 33-44 "An exemplary integrated circuit...one or more random access memories (RAM) 830").

96. [4]-"**(iii) memory interface configuration"** is disclosed by Dangelo'678 at Column 9 line 27 "interface requirements".

97. [5]-"**(iv) system architecture configuration"** is disclosed Dangelo'678 at Column 43 line 55 "architecture synthesis system".

98. [6]-**"receiving an identification of a location of at least one library file"** is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

99. [7]-**"generating through an automated process a customized description language model based on at least one customized parameter, the at least one prototype description, and the at least one extension logic description, the automated process including the acts of reading at least one prototype description and modifying the at least one prtotype description by substituting valures in the at least one prototype description or merging additional descriptions based on the at least one customized parameter"** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL", and at FIG 2 showing iterative modifications to the design ,and column 9 line 29 "Design Description. This is the functional description of the design and all its subsystem elements. The description is, ideally, given in a high level description language, such as VHDL. Depending on the nature of the design, the description can be entirely at the behavioral level, or it may be intertwined with an RTL description", and column 9 line 1 "The mega-cell and mega-function block 116 is chosen from pre-designed building block libraries, which are already designed for optimal performance" and FIG 12 "PREDESIGNED BLOCKS", and FIG 8 element 818 "LIBRARIES", and FIG 18 element 1810 "COMPONENT DATABASE".

100. Dangelo'678 does not expressly disclose 2 of the limitations.

101. [1]-**"selecting a process technology"** is disclosed by Gupte at Column 4 line 60 "process technology".

102. [2]-**"(i) processor instructions"** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

103. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Gupte and Wirthlin'434 to modify Dangelo'678. Starting with

Dangelo'678 as a basis for integrated circuit design, one of ordinary skill in the art would have been motivated to use Gupte to save time and money by using the same design program for various technologies, and to use Wirthlin'434 to save time by customizing the clock cycles to match the level of complexity of the instructions.

104. Claim 48 (Currently amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Dupenloup'123.

105. Claim 48 (Currently amended) is an independent "means for" claim with substantially the same limitations as Claim 40, thus is rejected for the same reasons.

106. Claim 60 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

107. Claim 60 (amended) is an independent method claim with 3 limitations.

108. [2]-**"generating, at a high level of abstraction, a processor specification based on one or more pre-defined instructions described in a hardware description language and including a user-definable portion based on the at least one user-defined extension description, the user-definable portion of said specification including at least one user-defined instruction having a function associated therewith"** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL", and at FIG 2 showing iterative modifications to the design ,and column 9 line 29 "Design Description. This is the functional description of the design and all its subsystem elements. The description is, ideally, given in a high level description language, such as VHDL. Depending on the nature of the design, the description can be entirely at the behavioral level, or it may be intertwined with an RTL description", and column 9 line 1 "The mega-cell and mega-function block 116 is chosen from pre-designed building block libraries, which are already designed for optimal performance" and FIG 12 "PREDESIGNED BLOCKS", and FIG 8 element 818 "LIBRARIES", and FIG 18 element 1810 "COMPONENT DATABASE".

109. [3]-**"based on said processor specification, generating a description of a hardware implementation of said configurable processor"** is disclosed by Dangelo'678 at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL", and at FIG 2 showing iterative modifications to the design ,and

column 9 line 29 "Design Description. This is the functional description of the design and all its subsystem elements. The description is, ideally, given in a high level description language, such as VHDL. Depending on the nature of the design, the description can be entirely at the behavioral level, or it may be intertwined with an RTL description", and column 9 line 1 "The mega-cell and mega-function block 116 is chosen from pre-designed building block libraries, which are already designed for optimal performance" and FIG 12 "PREDESIGNED BLOCKS", and FIG 8 element 818 "LIBRARIES", and FIG 18 element 1810 "COMPONENT DATABASE".

110. Dangelo'678 does not expressly disclose one limitation:

111. [1]-**"receiving an identification of one or more pre-defined instructions described in a hardware description language fore the configureable processor and at least one user-defined extension description, described in user-supplied hardware description language"** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

112. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to customize the timing to allow high-level instructions.

113. Claim 61 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

114. Claim 61 depends from Claim 60 (amended), with one additional limitation.

115. Dangelo'678 does not expressly disclose the additional limitation:

116. **generating a description including control logic necessary for the execution of said at least one user-defined instruction** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

117. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art

would have been motivated to do this to customize the timing to allow high-level instructions.

118. Claim 62 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

119. Claim 62 depends from Claim 61, with one additional limitation.

120. **instruction execution pipeline having a plurality of stages, said control logic including portions associated with said stages** is disclosed by Dangelo'678 at Column 27 line 22 "specific control elements are assigned to the control logic in the RT level description of the system".

121. Claim 63 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434 and Turino'892.

122. Claim 63 depends from Claim 60, with 3 additional limitations.

123. **(i)-registers** is disclosed by Dangelo'678 at Column 7 line 29 "registers".

124. **(iii)-scratchpad RAM** is disclosed by Dangelo'678 at Column 11 line 60 "RAM".

125. Dangelo does not disclose one limitation:

126. **(ii)-condition code choices** is disclosed by Turino'892 at Column 34 line 10 "Condition Code Register (CCR) - - 8 bits".

127. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 and Turino'892 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to customize the timing to allow high-level instructions, and to minimize the number of bits in the condition code register.

128. Claim 64 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434

129. Claim 64 depends from Claim 60, with 1 additional limitation.

130. **"at least one library of multimedia extensions"** is disclosed by Dangelo'678 at Column 9 line 2 "libraries".

131. Claim 65 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434

132. Claim 65 depends from Claim 60, with 1 additional limitation.

133. **"simulating said configurable processor"** is disclosed by Dangelo'678 at Column 4 line 15 "simulation".

134. Claim 66 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

135. Claim 66 depends from Claim 65, with 3 additional limitations.

136. **"running at least one script to generate simulation data"** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

137. **"running at least one simulation using at least said simulation data"** is disclosed by Dangelo'678 at Column 4 line 15 "simulation".

138. "determining the adequacy of said configurable processor based at least in part on said act of running" is disclosed by Dangelo'678 at Column 4 line 18 "This provides a check that the circuit implementation behaves as intended, and that the timing goals are achieved.

139. Claim 67 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434

140. Claim 67 depends from Claim 60, with 1 additional limitation.

141. "synthesizing said configurable processor using at least said description" is disclosed by Dangelo'678 at Column 4 line 6 "synthesis".

142. Claim 68 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

143. Claim 68 depends from Claim 67, with 2 additional limitations.

144. **"running at least one synthesis script to generate synthesis data"** is disclosed by Dangelo'678 at Column 14 line 20 "script shells and a command line".

145. "evaluating the adequacy of said synthesis data based at least in part on at least one design criterion" is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

146. Claim 69 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

147. Claim 69 depends from Claim 68, with 2 additional limitations.

148. **"at least one processor die size criterion"** is disclosed by Dangelo'678 at Column 41 line 46 "die size".

149. Dangelo'678 does not expressly disclose one limitation:

150. **"at least one specific processor performance criterion"** is disclosed by Wirthlin'434 at Column 10 line 36 "The custom-instruction sequence allows additional cycles for instructions that need significantly more time than traditional low-level instructions".

151. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wirthlin'434 to modify Dangelo'678. One of ordinary skill in the art would have been motivated to do this to customize the timing to allow high-level instructions.

152. Claim 70 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

153. Claim 70 depends from Claim 68, with 3 additional limitations.

154. **"revising at least one design element when said act of evaluating indicates that said synthesis data is not adequate"** is disclosed by Dangelo'678 at Column 5 line 32 "design is resynthesized until a design is arrived at that meets timing constraints".

155. **"re-running said at least one synthesis script using said at least one revised design element to generate revised synthesis data"** is disclosed by Dangelo'678 at Column 5 line 32 "design is resynthesized until a design is arrived at that meets timing constraints".

156. **"and re-evaluating the adequacy of said revised synthesis data based at least in part on said at least one design criterion"** is disclosed by Dangelo'678 at Column 5 line 32 "design is resynthesized until a design is arrived at that meets timing constraints".

157. Claim 71 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

158. Claim 71 depends from Claim 70, with 2 additional limitations.

159. **"at least one processor die size criterion"** is disclosed by Dangelo'678 at Column 41 line 46 "die size".

160. **"revising at least one library"** is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

161. Claim 72 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

162. Claim 72 depends from Claim 71, with 2 additional limitations.

163. **"at least one processor die size criterion"** is disclosed by Dangelo'678 at Column 41 line 46 "die size".

164. **"revising at least one control file"** is disclosed by Dangelo'678 at Column 27 line 22 "control elements".

165. Claim 73 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

166. Claim 73 depends from Claim 70, with 2 additional limitations.

167. **"processor clock speed"** is disclosed by Dangelo'678 at Column 10 line 52 "length of clock cycle"

168. **"at least one library"** is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

169. Claim 74 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Wirthlin'434.

170. Claim 74 depends from Claim 70, with 2 additional limitations.

171. **"processor power consumption"** is disclosed by Dangelo'678 Column 19 line 47 "allows the user to perform a "what if" analysis for choosing a preferred design in terms of size, speed, performance, technology, and power".

172. **"at least one netlist (net load)"** is disclosed by Dangelo'678 Column 49 line 56 "compiling and simulating the netlist".

173. Claim 75 (currently amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo'678 in view of Gupte and MPEP 2144.04(III) Legal Precedent.

174. Independent claim 75 (new) is a method claim with 8 limitations.

175. [1]-**"providing an existing processor core configuration"** is disclosed by Dangelo'678 at Column 5 line 32 "design is resynthesized until a design is arrived at that meets timing constraints". Also see Dangelo'678 FIG 2 which illustrates the iterative nature of integrated circuit design.

176. [2]-**"receiving one or more inputs from a user for at least one cutstomeized parameter of the exisiting processor core configuration for the integrated circuit device, the input being selected from a set of input parameters associated with said configuration, said parameters comprising: (i) at least one custom instruction"** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line", and at Column 14 line 21 "dc-shell script and constraints files", and at Column 3 line 49 "First, the designer specifies the desired behavior of the device in a high-level language, such as VHDL", and at FIG 2 showing iterative modifications to the design.

177. [5]-**"receiving an identification of a location of one or more library files"** is disclosed by Dangelo'678 at FIG 8 element 818 "CDE/SY LIBRARIES".

178. [7]-"a **customized description language model"** is disclosed by Dangelo'678 at Column 14 line 20 "interacts with the MDE programs via script shells and a command line" and at Column 14 line 21 "dc-shell script and constraints files".

179. Dangelo'678 does not explicitly disclose the additional limitations.

180. [3]-**"(ii) a cache configuration"** is disclosed by Gupte at Column 6 line 18 "cache memory".

181. [4]-**"(iii) a memory interface configuration"** is disclosed by Gupte at Column 6 line 18 "cache memory".

182. [6]-**"generating through an automated process"** is disclosed by MPEP 2144.04(III) Legal Precedent. *In re Venner*, 262 F.2d 91, 95, 120 USPQ 192, 194 (CCPA 1958) states "it is well settled that it is not "invention" to broadly provide a mechanical or automatic means to replace manual activity which has accomplished the same result." Additionally, MPEP 2144.04(III) states "broadly providing an automatic or mechanical means to replace a manual activity which accomplished the same result is not sufficient to distinguish over the prior art."

183. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use MPEP 2144.04(III) Legal Precedent to modify Dangelo'678. One of ordinary skill in the art would begin with Dangelo as a basis for designing integrated circuits, and then would be motivated to save time and money by carefully documenting and saving

modules of building blocks, or medium sized circuits that can be used repeatedly as building blocks for large designs. Note that this is analogous to using "libraries" of gate level components, rather than repeatedly designing similar gate level components. Additionally, one of ordinary skill in the art would be motivated to save time and money (and reduce error) by automating the repetitive steps of reading, substituting, or merging the relevant building blocks.

184. Claims 70-117 are rejected under 35 USC 103(a).

185. Claims 70-117 contain the same limitations as claims 12-22, 40-42, and 47-48, and 60-74 above, and thus are rejected for the same reasons.

Conclusion

186. All pending claims are rejected under 35 USC 103.

187. The Examiner requests (for the second time) the following: (1) the **earliest User's Manual for the Architect™** product which is the embodiment of the instant claimed invention, including a mapping of claim limitations to the product features, (2) all relevant information regarding the **first publication, public use, or sale of said product.** This information is important to evaluate the assertions of commercial success, and important to evaluate potential statutory bars.

188. It is possible that the substantial detail in the specification contains patentable subject matter, in the nature of an expert system for facilitating integrated circuit design.

189. The declaration is some evidence of commercial success, and is given some weight. Please see *Minnesota Mining* regarding what type of evidence would be given great weight.

Communication

190. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Tuesday through Friday from 9:00 AM to 8:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone number for this group is 703-872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

* * * *


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